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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/616,012	07/08/2003	Daniel Mark Dreps	AUS20010256US2	1050

23504 7590 12/01/2004

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EXAMINER	
WELLS, KENNETH B	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 12/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/616,012	DREPS ET AL.	
	Examiner	Art Unit	
	Kenneth B. Wells	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 October 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☒ Claim(s) *18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. The amendment filed on 10/8/04 has been received and entered in the case. In view of the arguments included therein, the previous rejection based on Andoh et al is hereby withdrawn by the examiner, as is the provisional double-patenting rejection. However, new grounds of rejection are set forth in view of alternative interpretations of the prior art of record.

2. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

3. Claim 7 is objected to because of the following informalities: the amendment on line 4, to change "comprising" to --comprises-- is incorrect. Appropriate correction is required.

4. Claims 1-15 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

It is misdescriptive, and thus indefinite, to recite the reference combiner and single-ended comparator as separate elements in claim 1, because the reference combiner is part of the single-ended comparator, i.e., as understood by the

examiner, the recited reference combiner is the combination of FETs N11 and N12 in instant Fig. 3B, whereas the single-ended comparator is the entire Fig. 3B circuitry. Note the same problem in claim 10 concerning the separate steps of combining and comparing, which is not consistent with what is shown in instant Fig. 3B. Also indefinite in the above-noted claims is the "differential comparator" because it cannot be determined if this is referring to the combination of FETs N11 and N12 in instant Fig. 3B, or if it is referring to the Fig. 3A circuitry. This ambiguity should be cleared up in response to this office action.

5. Claims 1-6, 8-14, 16 and 17 are rejected under 35 U.S.C. 102(b) as being anticipated by Andoh et al.

Note Fig. 1, where the recited pair of differential inputs reads on the gates of FETs 8, 9; the recited single-ended input reads on the gate of FET 11; the recited reference combiner and single-ended comparator read on the combination of FETs 8, 9 and 11; the differential comparator reads on the FETs 8, 9; and the single-ended comparator reads on FET 11. The recitation of the "single-ended data signal" (claims 1 and 10) is met because FET 11 in Andoh et al is capable of receiving such a data input signal (merely intended use), as pointed out during the

telephonic interview of 9/29/04. The first through third controlled current sources are FETs 8, 9 and 11, respectively (or 9, 8 and 11, respectively). The fixed current source of claims 5 and 9 reads on FET 12, and the recited first resistance of claim 6 reads on diode-connected FET 10. The comparing of the single-ended signal to the reference value occurs when the differential input is applied to the gates of FETs 8 and 9 at the same time the reference signal is applied to the gate of FET 11 (the "second comparing" recited in claim 10 occurs when the differential input is applied to the gates of FETs 8 and 9). The steps of claims 11-14 are all deemed to be inherent during the operation of Fig. 1 of Andoh et al because the claimed structure and circuitry shown in instant Fig. 3B is the same as that illustrated in Fig. 1 of Andoh et al. The limitations of claims 16 and 17 are seen to be essentially the same as those noted above and thus are all anticipated as well.

6. Claims 1-6, 8-14, 16 and 17 are rejected under 35 U.S.C. 102(b) as being anticipated by Alexander et al.

Note Fig. 4, where the recited pair of differential inputs reads on the gates of FETs 52 and 80 (or at the gates of FETs 58 and 82); the recited single-ended input reads on the gate of FET 54 (or the gate of FET 56); the recited reference combiner

reads on the combination of FETs 52 and 80 (or the combination of FETs 58 and 82); the differential comparator reads on the combination of FETs 52 and 80 (or the combination of FETs 58 and 82); and the single-ended comparator reads on the combination of FETs 52, 54 and 80 (or the combination of FETs 56, 58 and 82, or just FET 54 by itself or just FET 56 by itself. The recited first through third controlled current sources read on FETs 52, 80 and 54, respectively (or FETs 58, 82 and 56, respectively). The fixed current source of claims 5 and 9 reads on either current source 60 or current source 62. The recited first through third transistors are FETs 80, 52 and 54, respectively (or FETs 82, 58 and 56, respectively). The recited first resistance reads on element 68 (it is connected to the source of FET 54 through FET 52). The comparing of the single-ended signal to the reference value occurs when the differential input is applied to the gates of FETs 52 and 80 at the same time the reference signal is applied to the gate of FET 54 (the "second comparing" recited in claim 10 occurs when the differential input is simultaneously applied to the gates of FETs 58 and 82). The steps of claims 11-14 are all deemed to be inherent during the operation of Fig. 1 of Andoh et al because the claimed structure and circuitry shown in instant Fig. 3B is the same as that illustrated in Fig. 4 of Alexander et al. The limitations

of claims 16 and 17 are seen to be essentially the same as those noted above and thus are all anticipated as well.

7. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Alexander et al.

The recited fourth and fifth transistors read on FETs 58 and 82, respectively; and the recited second resistance reads on element 70 (it is connected to the source of FET 82 through FET 58). The limitation that the gain of the differential comparator is the same as that of the single-ended comparator, though not disclosed, nevertheless would have been obvious to those having ordinary skill in the art who will easily recognize that Fig. 4 is a balanced circuit with the sizes of the transistors, current sources on the left hand side of Fig. 4 needing to be equal to those on the right hand side (in order to produce balanced differential output signal Vo).

8. Claim 15 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Claim 18 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent

form including all of the limitations of the base claim and any intervening claims.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kenneth B. Wells whose telephone number is (571)272-1757. The examiner can normally be reached on Monday through Friday from 8:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy P. Callahan, can be reached at (571)272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Kenneth B. Wells
Primary Examiner
Art Unit 2816

November 26, 2004